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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,467	07/24/2003	Anthony L. Priborsky	STL11301	1329

27365 7590 05/25/2010

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EXAMINER	
PHAN, MAN U	
ART UNIT	PAPER NUMBER
2475	

MAIL DATE	DELIVERY MODE
05/25/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/626,467	PRIBORSKY, ANTHONY L.	
	Examiner	Art Unit	
	Man Phan	2475	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-13,16-20 and 23-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 7-11, 13, 16-19, 23-26* is/are rejected.

7)☒ Claim(s) *12 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment and Argument

1. This communication is in response to applicant's 3/22/2010 Amendment in the application of Priborsky for the "Methods Dynamic control of physical layer quality on a serial bus" filed 07/24/2003. This application is a Request for Continued Examination (RCE) under 37 C.F.R. 1.114 filed on Sept. 24, 2009. The proposed amendment and response has been entered and made of record. Claims 1-4, 7-13, 16-20 and 23-26 are pending in the application.

2. Applicant's remarks and argument to the rejected claims are insufficient to distinguish the claimed invention from the cited prior arts or overcome the rejection of said claims under 35 U.S.C. 103 as discussed below. Applicant's argument with respect to the pending claims have been fully considered, but they are not persuasive for at least the following reasons.

3. In response to Applicant's argument that the reference does not teach or reasonably suggest the functionality upon which the Examiner relies for the rejection. The Examiner first emphasizes for the record that the claims employ a broader in scope than the Applicant's disclosure in all aspects. In addition, the Applicant has not argued any narrower interpretation of the claim limitations, nor amended the claims significantly enough to construe a narrower meaning to the limitations. Since the claims breadth allows multiple interpretations and meanings, which are broader than Applicant's disclosure, the Examiner is required to interpret the claim limitations in terms of their broadest reasonable interpretations while determining patentability of the disclosed invention. See MPEP 2111. In other words, the claims must be

given their broadest reasonable interpretation consistent with the specification and the interpretation that those skilled in the art would reach. See *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000), *In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999), and *In re American Academy of Science Tech Center*, 2004 WL 1067528 (Fed. Cir. May 13, 2004). Any term that is not clearly defined in the specification must be given its plain meaning as understood by one of ordinary skill in the art. See MPEP 2111.01. See also *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989), *Sunrace Roots Enter. Co. v. SRAM Corp.*, 336 F.3d 1298, 1302, 67 USPQ2d 1438, 1441 (Fed. Cir. 2003), *Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1298 67 USPQ2d 1132, 1136 (Fed. Cir. 2003). The interpretation of the claims by their broadest reasonable interpretation reduces the possibility that, once the claims are issued, the claims are interpreted more broadly than justified. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). Also, limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)*. Therefore, the failure to significantly narrow definition or scope of the claims and supply arguments commensurate in scope with the claims implies the Applicant intends broad interpretation be given to the claims. The Examiner has interpreted the claims in parallel to the Applicant in the response and reiterates the need for the Applicant to distinctly define the claimed invention.

4. Applicant's argument with respect to the rejected claims that the cited references fail to teach or suggest the novel concept of the "*physical layer quality* " in communication system. However, the reference are applied herein for the teaching of the novel methods and system for

controlling a PHY layer of user data transmitted between first and second ends of a serial bus (*controlling the PHY layer quality of service*). The Applicant's attention is directed to Fig. 2 of Ghaffari (US#6,829,663) for the teaching of controlling the PHY layer properties between a storage device and a host computer system (*controlling the PHY layer quality of the serial bus*). Ghaffari (US#6,829,663) does in fact teach in Fig. 2 a link layer (132) and the PHY (136) in which the link layer 132 performs primitive coding functions (*layer 132 is provided with a primitive decoder 212 and a primitive encoder 216*), and a link control state machine 232 is provided for controlling the operation of the link layer 132 (*controlling the PHY layer quality utilizing primitive coding functions*). Furthermore, Fig. 4 is a flow chart illustrating the steps taken in connection with the flow of data through an adapter, in which at step 408, primitives received are decoded using the primitive decoder 312 (*control PHY layer quality using primitive data*); at step 412, the data is placed on the link transport data bus (i.e. the parallel data channel 140b interconnecting the link layer and the transport layer). Data is then presented to the transport (step 416). The transport then provides the data to the host interface 124, with data buffering if necessary (step 420). In the same field of endeavor, Lo (US#2004/0010625) teaches in FIG. 3 is a block diagram of the interface device used for the synchronous transfer of data over serial ATA, in which the link layer portion 34 generates some primitives indicating the state of the layer portion 34 by link state machine (*for controlling the PHY layer quality of the communication channels*). The status monitor 361 continues to detect the status of the link layer portion 34. The fix pattern generator 362 generates primitive formats responding to the status of the link layer portion 34 detected by the status monitor 361, such as XRDY and RRDY. The

physical layer controller 363 directly returns the primitive formats to the device 30 without receiving the primitive formats to the link layer portion ([0022]-[0023]).

Since no substantial amendments have been made and the Applicant's arguments are not persuasive, the claims are drawn to the same invention and the text of the prior art rejection can be found in the previous Office Action. Therefore, the Examiner maintains that the references cited and applied in the last office actions for the rejection of the claims are maintained in this office action.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 7-11, 13, 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghaffari et al. (US#6,829,663) in view of Lo et al. (US#2004/0010625).

Regarding claims 1, 3, 10, the references disclose a novel system and method for controlling a PHY layer quality of user data transmitted between first and second ends of a serial bus, according to the essential features of the claims. Ghaffari et al. (US#6,829,663) discloses an interface device (104) for the synchronous transfer of data over serial ATA (116), comprising: a link layer portion (132) for receiving the data from a device (Ghaffari discloses frames of data are passed between the link layer 132 and the physical layer 136, and between the physical layer 136 and the serial device 116 as 10B/8B encoded data, since it is duplex communications,

inherently the link layer would also receive data from the serial device; col. 6: lines 6-9); and a physical layer portion (136); a status monitor (232) for detecting the status of the link layer portion (col. 6: lines 24-25); a fix pattern generator (212, 216) for providing primitive formats responding to the status of the link layer portion (e.g., performing either primitive coding or encoding depending on the status of the link layer; col. 6: lines 9-14); and a physical layer controller (136) for directly returning the primitive formats to the device without receiving the primitive formats to the link layer portion (Ghaffari discloses frames of data passed between the physical layer 136 and the serial device 115 as 10B/8B encoded data; col. 6: lines 6-8).

However, Ghaffari does not explicitly disclose the physical layer portion comprising a status monitor, a fix pattern generator, and a physical controller. In the same field of endeavor, Lo et al. (US#2004/0010625) teaches in Fig. 3 a block diagram illustrated the physical portion includes a status monitor (361), a fix pattern generator (362), and a physical layer controller (363), in which the link layer portion 34 generates some primitives indicating the state of the layer portion 34 by link state machine. The status monitor 361 continues to detect the status of the link layer portion 34. The fix pattern generator 362 generates primitive formats responding to the status of the link layer portion 34 detected by the status monitor 361, such as XRDY and RRDY. The physical layer controller 363 directly returns the primitive formats to the device 30 without receiving the primitive formats to the link layer portion ([0023] plus). High Performance Serial Bus has been in practical use widely, thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to use Lo's method of transferring data over a serial bus in Ghaffari's system so that high speed communication between any node device can be achieved.

Regarding claims 2, 4, 11, 13, Ghaffari- Lo disclose the claimed invention as described above. Ghaffari also discloses the link controller for controlling the PHY layer in real time (Col. 4: lines 22-34; Col. 4, lines 63 - Col. 5, line 2).

Regarding claims 7-9, 16-18, Ghaffari- Lo disclose the claimed invention as described above. Furthermore, in a computer system, functional devices such as disc drives and disc drive controllers in a host computer system are typically connected by transceivers to a transmission line and various connectors that serve as a serial bus are well known in the art of communications control system.

One skilled in the art of communications would recognize the need for controlling a PHY layer of user data transmitted between first and second ends of a serial bus, and would apply Lo's novel use of a interface device for the synchronous transfer of data over serial ATA into Ghaffari's operating layers of an adapter interconnected to a computer system. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Lo's interface device and method for transferring data over serial ATA into Ghaffari's method and apparatus for the synchronous control of a serial interface with the motivation being to provide a system and method for dynamic control of physical layer quality on a serial bus.

7. Claims 19, 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghaffari et al. (US#6,829,663) in view of Lo et al. (US#2004/0010625).

Regarding claims 19, 24, 26, the references disclose a novel system and method for controlling a PHY layer of user data transmitted between first and second ends of a serial bus,

according to the essential features of the claims. Ghaffari et al. (US#6,829,663) discloses an interface device (104) for the synchronous transfer of data over serial ATA (116), comprising: a link layer portion (132) for receiving the data from a device (Ghaffari discloses frames of data are passed between the link layer 132 and the physical layer 136, and between the physical layer 136 and the serial device 116 as 10B/8B encoded data, since it is duplex communications, inherently the link layer would also receive data from the serial device; col. 6: lines 6-9); and a physical layer portion (136); a status monitor (232) for detecting the status of the link layer portion (col. 6: lines 24-25); a fix pattern generator (212, 216) for providing primitive formats responding to the status of the link layer portion (e.g., performing either primitive coding or encoding depending on the status of the link layer; col. 6: lines 9-14); and a physical layer controller (136) for directly returning the primitive formats to the device without receiving the primitive formats to the link layer portion (Ghaffari discloses frames of data passed between the physical layer 136 and the serial device 115 as 10B/8B encoded data; col. 6: lines 6-8).

However, Ghaffari does not explicitly disclose the physical layer portion comprising a status monitor, a fix pattern generator, and a physical controller. In the same field of endeavor, Lo et al. (US#2004/0010625) teaches in Fig. 3 a block diagram illustrated the physical portion includes a status monitor (361), a fix pattern generator (362), and a physical layer controller (363), in which the link layer portion 34 generates some primitives indicating the state of the layer portion 34 by link state machine. The status monitor 361 continues to detect the status of the link layer portion 34. The fix pattern generator 362 generates primitive formats responding to the status of the link layer portion 34 detected by the status monitor 361, such as XRDY and RRDY. The physical layer controller 363 directly returns the primitive formats to the device 30

without receiving the primitive formats to the link layer portion ([0023] plus). High Performance Serial Bus has been in practical use widely, thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to use Lo's method of transferring data over a serial bus in Ghaffari's system so that high speed communication between any node device can be achieved.

Regarding claims 23, 25, Ghaffari- Lo disclose the claimed invention as described above. Furthermore, in a computer system, functional devices such as disc drives and disc drive controllers in a host computer system are typically connected by transceivers to a transmission line and various connectors that serve as a serial bus are well known in the art of communications control system.

One skilled in the art of communications would recognize the need for controlling a PHY layer of user data transmitted between first and second ends of a serial bus, and would apply Lo's novel use of a interface device for the synchronous transfer of data over serial ATA into Ghaffari's operating layers of an adapter interconnected to a computer system. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Lo's interface device and method for transferring data over serial ATA into Ghaffari's method and apparatus for the synchronous control of a serial interface with the motivation being to provide a system and method for dynamic control of physical layer quality on a serial bus.

Allowable Subject Matter

8. Claims 12, 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is an examiner's statement of reasons for the indication of allowable subject matter: The closest prior art of record fails to disclose or suggest wherein the quality sensing circuit comprises: a physical layer quality sensor sensing the received first signal; a quality standard; and a quality compare circuit comparing the received first signal to the quality standard and providing the control primitive data; wherein further comprising a second apparatus controlling a second physical layer quality in a direction on the serial bus that is opposite to the direction, to provide bi-directional physical layer quality control on the serial bus, as specifically recited in the claims.

Conclusion

10. **THIS ACTION THIS ACTION IS MADE FINAL**. See MPEP ' 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this

final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Phan whose telephone number is (571) 272-3149. The examiner can normally be reached on Mon - Fri from 6:00 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dang Ton, can be reached on (571) 272-3171. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at toll free 1-866-217-9197.

Mphan

May 21, 2010

/Man Phan/

Primary Examiner, Art Unit 2475

Search Notes (continued)

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/626,467	PRIBORSKY, ANTHONY L.	
Examiner	**Art Unit**	
Man Phan	2475	

SEARCHED			
Class	Subclass	Date	Examiner
370	241-254	5/20/2010	MP
	493-527		MP
375	221-229		MP
709	204-224		MP
713	300-323		MP

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST/WEST search update (search 370, 375, 709-713 classes)	5/20/2010	MP